Reliability Report

General Information	
Product Line	*U371*
Product Description	*HIGH VOLTAGE GATE DRIVER*
Product division	*I&PC*
Package	*SO8*
Silicon process technology	*BCD OFF LINE*

Locations	
Wafer fab location	*AMK*
Assembly plant location	*ST SHENZHEN CHINA*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	01-dec-2016	10	G. D'Angelo	Original document
2.0	24-Feb-17	11	G. D'Angelo	Updated with Package Oriented test on U371 device

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U371 device diffused in AMK and assembled in SO8 in ST SHENZHEN CHINA in the overall plan of LeadFrame change in Shenzhen.

Considering that U371 device is assembled in the same plant with the same package and the same leadframe of U324, the positive results obtained from U324 can be extended to U371 device.

According to Reliability Qualification Plan, below is the list of the overall trials performed on samples with new LeadFrame:

Die Oriented Tests (on U324 device)

- High Temperature Operating Life
- Early Life Failure Rate

Package Oriented Tests (on U324 device)

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias
-

Package Oriented Tests (on U371 device)

- Preconditioning
- Temperature Cycling

Electrical Characterization (on U371 device)

- ESD resistance test
- LATCH-UP resistance test

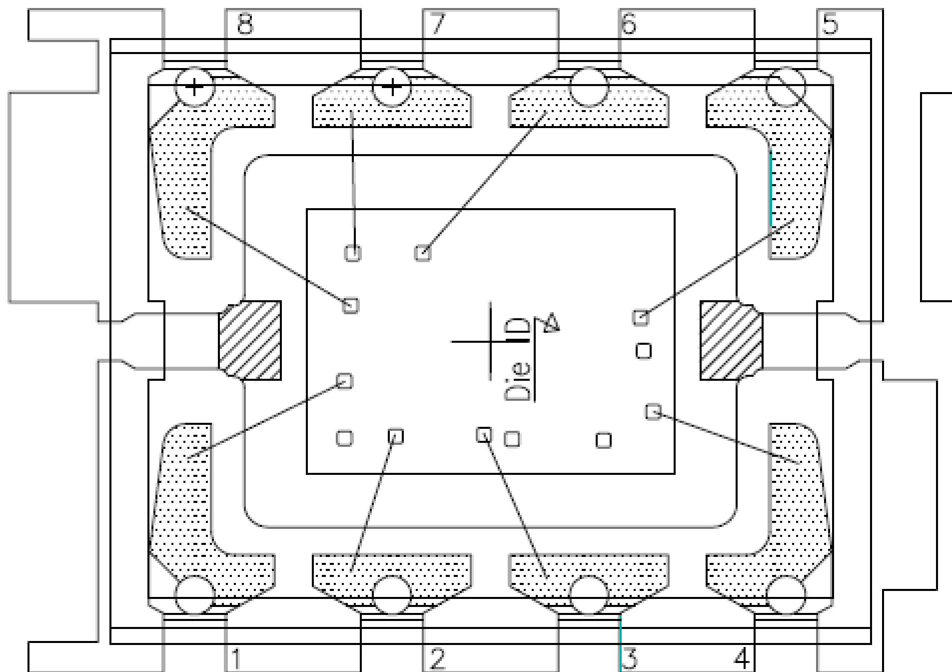
2.2 Conclusion

Taking in account the results of the trials performed **the U371 diffused in AMK and assembled in SO8 in ST SHENZHEN CHINA can be qualified from reliability viewpoint.**

3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Bonding Diagram



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AMK*
Wafer diameter	*6 inches*
Wafer thickness	*375um*
Silicon process technology	*BCD OFF LINE*
Die finishing back side	*Cr/Ni*
Die size	*2370x1700 um*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*ST SHENZHEN CHINA*
Package description	*SO8*
Molding compound	*G700*
Wires bonding materials/diameters	*Cu/1 mils*
Die attach material	*8601*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Rev.
1	AEA (U324 device)
2	AEA (U324 device)
3	AEA (U324 device)
4	BC6 (U371 device)

4.2 Test plan and results summary

Die Oriented Tests (performed on U324 assembled in Shenzhen in SO8 package)

Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
HTOL	High Temperature Operating Life						
	PC before	**Tj=150°C, VCC=17V**	**0/77**	**0/77**	**0/77**	**1000h**	
ELFR	Early Life Failure Rate						
		Tj=150°C, VCC=17V	**0/800**	**0/800**	**0/800**	**24h**	

Package Oriented Tests (performed on U324 assembled in Shenzhen in SO8 package)

Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	**0/231**	**0/231**	**0/231**		
THB	Temperature Humidity Bias						
	PC before	**Ta=85°C/85%RH VCC=17V**	**0/77**	**0/77**	**0/77**	**1000h**	
AC	Autoclave						
	PC before	**121°C 2atm**	**0/77**	**0/77**	**0/77**	**96h**	
TC	Temperature Cycling						
	PC before	**Temp. range: -50/+150°C**	**0/77**	**0/77**	**0/77**	**2000cy**	
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**0/45**	**0/45**	**--**	**1000h**	

Package Oriented Tests (performed on U371)

Test	Method	Conditions	Failure/SS	Duration	Note
			Lot 4		
PC3	Pre-Conditioning: Moisture sensitivity level 3				
		192h 30°C/60% - 3 reflow PBT 260°C	**0/77**		
PC1	Pre-Conditioning: Moisture sensitivity level 1				
		168h 85°C/85% - 3 reflow PBT 260°C	**0/77**		
TC	Temperature Cycling				
	PC3 before	**Temp. range: -50/+150°C**	**0/77**	**1000cy**	
TC	Temperature Cycling				
	PC1 before	**Temp. range: -50/+150°C**	**0/77**	**1000cy**	

Electrical Characterization Tests (performed on U371)

Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results
ESD	Electro Static Discharge (performed on SO8)					
	Human Body Model	**+/- 2kV**	**3**	1		**PASSED**
	Machine Model	**+/- 200V**	**3**	1		**PASSED**
	Charge Device Model	**+/- 500V (+/-750V on corner pins)**	**3**	1		**PASSED**
LU	Latch-Up (performed on PDIP)					
	Over-voltage and Current Injection	**Tamb=25°C Jedec78**	**6**	1		**PASSED**

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 Early Life Failure Rate

This test is to evaluate the defects inducing failure in early life.
The device is stressed in biased conditions at the max junction temperature.

The read-outs flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing (24 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs or 240hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168hrs or 240hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011

Reliability Report

General Information	
Product Line	*U332*
Product Description	*HV Driver for Intelligent Power Module*
Product division	*I&PC*
Package	*SO16*
Silicon process technology	*BCD OFF LINE*

Locations	
Wafer fab location	*Ang Mo Kio AMK6*
Assembly plant location	*ST SHENZHEN CHINA*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	22-Nov-16	12	G. D'Angelo	Original document

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5.3.1 Latch-up 12
5.3.2 E.S.D. 12

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U332 device diffused in Ang Mo Kio AMK6 and assembled in SO16 in ST SHENZHEN CHINA in the overall plan of LeadFrame change in Shenzhen.

According to Reliability Qualification Plan, below is the list of the overall trials performed on samples with new LeadFrame:

Package Oriented Tests

- Preconditioning
- Temperature Cycling

2.2 Conclusion

Taking in account the results of the trials performed **the U332 diffused in Ang Mo Kio AMK6 and assembled in SO16 in ST SHENZHEN CHINA can be qualified from reliability viewpoint.**

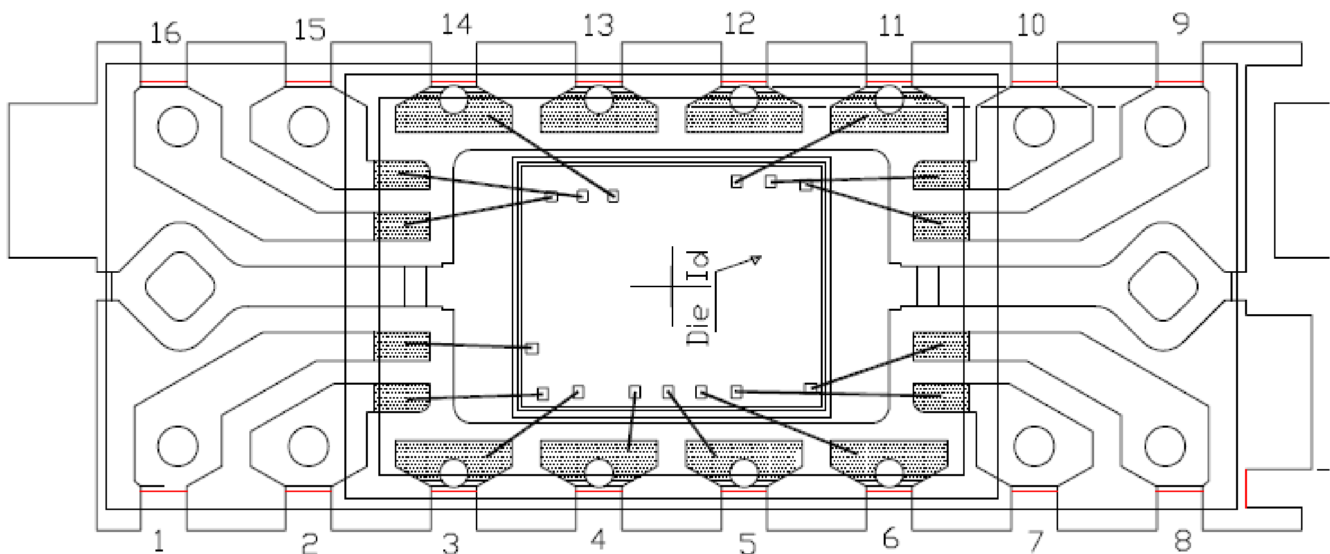
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Bonding diagram

MBD Line"U332" – SHENZHEN (3068)
PKG:"Q7"(SO 16)

FRAME PAD : $\frac{94 \times 150 \text{ mls}}{2{,}390 \times 3{,}810 \text{ mm}}$



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*Ang Mo Kio AMK6*
Wafer diameter	*6 inches*
Wafer thickness	*375um*
Silicon process technology	*BCD OFF LINE*
Die finishing back side	*Cr/Ni/Au*
Die size	*2390x1950 um*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*ST SHENZHEN CHINA*
Package description	*SO16*
Molding compound	*G630*
Wires bonding materials/diameters	*Cu/1 mils*
Die attach material	*8601*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Revision
1	AG6

4.2 Test plan and results summary

Package Oriented Tests					
Test	**Method**	**Conditions**	**Failure/SS**	**Duration**	**Note**
			Lot 1		
PC	Pre-Conditioning: Moisture sensitivity level 3				
		192h 30°C/60% - 3 reflow PBT 260°C	**0/77**		
TC	Temperature Cycling				
	PC before	**Temp. range: -50/+150°C**	**0/77**	**1000cy**	

Considering that U332 device is in same technology of the U329 device (assembled in Shenzhen in SO16 package) the positive results obtained from U329 device can be extended to U332 device.
Data of U332 version assembled in Muar are also considered.

Die Oriented Tests (performed on U332 assembled in SO16 in Muar)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results**
HTOL	High Temperature Operating Life					
	PC before	**Tj=150°C Vcc=20V, VHV=580V**	**77 40**	1 2	**1000h**	**PASSED**
HTRB	High Temperature Reverse Bias					
		Tj=150°C Vhv=630V,Vcc=21V	**77**	3	**1000h**	**PASSED**

Package Oriented Tests (performed on U329 assembled in SO16 in Shenzhen)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Note**
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30°C/60% - 3 reflow PBT 260°C	**0/231**	1		**PASSED**
THB	Temperature Humidity Bias					
	PC before	**Ta=85°C/85%RH HV=100V, Vcc=20V**	**0/77**	1	**1000h**	**PASSED**
AC	Autoclave					
	PC before	**121°C 2atm**	**0/77**	1	**168h**	**PASSED**
TC	Temperature Cycling					
	PC before	**Temp. range: -50/+150°C**	**0/77**	1	**1000cy**	**PASSED**
HTSL	High Temperature Storage					
	No bias	**Tamb=150°C**	**0/77**	1	**1000h**	**PASSED**

Electrical Characterization Tests (performed on U332 assembled in SO16 in Muar)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results**
ESD	Electro Static Discharge (SO8 package)					
	Human Body Model	**+/- 2kV – all pins**	**3**	1		**PASSED**
	Machine Model	**+/- 200V all pins except pins 14-15-16(HV pins) +/- 100V - pins 14-15-16(HV pins)**	**3**	1		**PASSED**
	Charge Device Model	**+/- 1500V**	**3**	1		**PASSED**
LU	Latch-Up (on PDIP package)					
	Over-voltage and Current Injection	**Tamb=85°C Jedec78**	**6**	1		**PASSED**

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing at 168 and 500 hrs @ Ta=25°C
- Final Testing @ 1000 hrs @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing @ 168 and 500 hrs @ Ta=25°C
- Final Testing @ 1000 hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Testing @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing @168 hrs @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 2000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing @ 168 and 500hrs @Ta=25°C
- Testing @ 1000 hrs @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
CDF-AEC-Q100-011

Reliability Report

General Information	
Product Line	*U338*
Product Description	*HV Resonant Controller*
Product division	*I&PC*
Package	*SO16*
Silicon process technology	*BCD OFF LINE*

Locations	
Wafer fab location	*AMK*
Assembly plant location	*ST SHENZHEN CHINA*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	22-Nov-16	12	G. D’Angelo	Original document

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
0061692	: Reliability tests and criteria for qualifications

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of U338 device diffused in AMK and assembled in SO16 in ST SHENZHEN CHINA in the overall plan of LeadFrame change in Shenzhen.

According to Reliability Qualification Plan, below is the list of the overall trials performed on samples with new LeadFrame:

Package Oriented Tests

- Preconditioning
- Temperature Cycling

2.2 Conclusion

Taking in account the results of the trials performed **the U338 diffused in AMK and assembled in SO16 in ST SHENZHEN CHINA can be qualified from reliability viewpoint.**

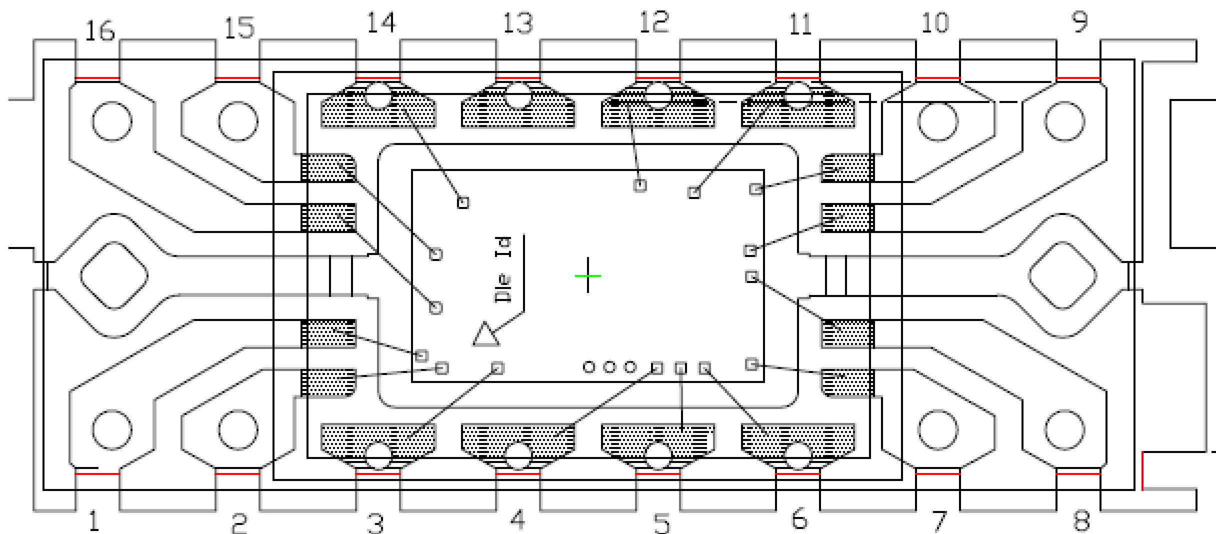
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Bonding diagram

MBD Line"U338" – SHENZHEN (3068)
PKG:"Q7"(SO 16)

FRAME PAD : 94 x 150 mls / 2,390 x 3,810 mm



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AMK*
Wafer diameter	*6 inches*
Wafer thickness	*375um*
Silicon process technology	*BCD OFF LINE*
Die finishing back side	*Cr/Ni*
Die size	*3200x1930 um*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*ST SHENZHEN CHINA*
Package description	*SO16*
Molding compound	*G630*
Wires bonding materials/diameters	*Cu/1 mils*
Die attach material	*8601*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Revision
1	AA6

4.2 Test plan and results summary

Package Oriented Tests					
Test	**Method**	**Conditions**	**Failure/SS Lot 1**	**Duration**	**Note**
PC3	Pre-Conditioning: Moisture sensitivity level 3				
		192h 30°C/60% - 3 reflow PBT 260°C	**0/77**		
TC	Temperature Cycling				
	PC before	**Temp. range: -50/+150°C**	**0/77**	**1000cy**	

Considering that U338 device is a metal change of the U329 device and this change is marginal from the reliability point of view. The positive results obtained from U329 assembled in Muar and Shenzhen assy plant can be extended to U338 device.

Die Oriented Tests (performed on U329, assembled in Muar)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results**
HTOL	High Temperature Operating Life					
	PC3 before	Tj=150°C, Vcc=16V, VHV=560V	77	1	1000h	PASSED
HTRB	High Temperature reverse Bias					
	PC1 before	Tj=150°C, Vcc=25V, VHV=600V	77	1	1000h	PASSED

Package Oriented Tests (performed on U329 assembled in SO16 in Shenzhen)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Note**
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30°C/60% - 3 reflow PBT 260°C	0/231	1		PASSED
THB	Temperature Humidity Bias					
	PC before	Ta=85°C/85%RH HV=100V, Vcc=20V	0/77	1	1000h	PASSED
AC	Autoclave					
	PC before	121°C 2atm	0/77	1	168h	PASSED
TC	Temperature Cycling					
	PC before	Temp. range: -50/+150°C	0/77	1	1000cy	PASSED
HTSL	High Temperature Storage					
	No bias	Tamb=150°C	0/77	1	1000h	PASSED

Electrical Characterization Tests (performed on U329 assembled in Muar)						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results**
ESD	Electro Static Discharge					
	Human Body Model	+/- 2kV on all pins except HV pins (#14,#15,#16) +/- 1kV on HV pins (#14,#15,#16)	3	1		PASSED
	Charge Device Model	+/- 1kV	3	1		PASSED
LU	Latch-Up					
	Over-voltage and Current Injection	Tamb=85°C Jedec78	6	1		PASSED

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance.
The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs or 240hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168hrs or 240hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Testing @ 168 and 500hrs
- Final Testing (1000 hr.) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less
IN high	-100mA	Inom+100mA	1.5 x VDD or MSV or AMR, whichever is less

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011